The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. **(Currently Amended)** A resistive memory device comprising:

a conductive bottom electrode;

a multi-resistive state element arranged on top of and in contact with the bottom electrode such that a bottom interface is created, the multi-resistive state element having a substantially crystalline layer that, while substantially maintaining its substantially crystalline structure, has a modifiable resistance; and

a conductive top electrode arranged on top of and in contact with the multi-resistive state element such that a top interface is created;

wherein the resistance of the resistive memory device may be changed by applying a first voltage having a first polarity across the conductive electrodes and reversibly changed by applying a second voltage having a second polarity across the conductive electrodes; and

wherein at least the top interface or the bottom interface is subjected to ~~a~~ **at least one** treatment **primarily** directed towards changing properties of the at least one interface.

2. (Original) The resistive memory device of claim 1, wherein:

the at least one treatment is an ion implant.

3. (Original) The resistive memory device of claim 1, wherein:

the at least one treatment is exposure to an anneal.

4. (Previously Presented) The resistive memory device of claim 3, wherein:

the anneal is performed while the multi-resistive state element is formed

5. (Original) The resistive memory device of claim 1, wherein:

the at least one treatment is exposure to a gas.

6. (Original) The resistive memory device of claim 1, wherein:

the at least one treatment is at least partially caused through deposition of an additional layer in one of the conductive electrodes.

7. (Original) The resistive memory device of claim 6, wherein:

the at least one treatment is completed with an anneal that causes a chemical reaction on the multi-resistive state element.

8. (Original) The resistive memory device of claim 7, wherein:

the anneal is performed after the bottom electrode is formed

9. (Original) The resistive memory device of claim 8, wherein:

the anneal is performed after the multi-resistive state element is formed

10. (Original) The resistive memory device of claim 9, wherein:

the anneal is performed after the top electrode is formed

11. (Original) The resistive memory device of claim 6, wherein:

the at least one treatment is completed with exposure to a gas that causes a chemical reaction in the multi-resistive state material.

12. (Original) The resistive memory device of claim 11, wherein:

the exposure is performed after the bottom electrode is formed

13 (Original) The resistive memory device of claim 12, wherein:

the exposure is performed after the multi-resistive state element is formed

14. (Original) The resistive memory device of claim 13, wherein:

the exposure is performed after the top electrode is formed

15. (Original) The resistive memory device of claim 6, wherein:

the deposition is performed by sputtering.

16. (Original) The resistive memory device of claim 6, wherein:

the deposition is performed by chemical vapor deposition.

17. (Original) The resistive memory device of claim 6, wherein:

the deposition is performed by evaporation.

18. (Original) The resistive memory device of claim 6, wherein:

the deposition is performed by atomic layer deposition.

19. (Original) The resistive memory device of claim 1, wherein:

the at least one treatment is caused by a chemical reaction between one of the electrodes and the multi-resistive state element.

20. (Original) The resistive memory device of claim 19, wherein:

an anneal process is a catalyst for the chemical reaction.

21. (Original) The resistive memory device of claim 19, wherein:

an exposure to a gas is a catalyst for the chemical reaction.

22. (Original) The resistive memory device of claim 1, wherein:

the at least one treatment is caused by a plasma process.

23. (Original) The resistive memory device of claim 22, wherein:

the plasma process is a plasma etch.

24. (Previously Presented) The resistive memory device of claim 1, wherein:

both the bottom interface and the top interface are subject to a treatment, the treatments being different from each other.

25. (Original) The resistive memory device of claim 1, wherein:

the at least one treatment is caused by re-sputtering.

26. (Original) The resistive memory device of claim 1, wherein:

the at least one treatment is caused the bombardment of inert ions.

27. (Previously Presented) The resistive memory device of claim 1, wherein:

the at least one treatment is caused by a laser treatment.

28. **(Currently Amended)** A resistive memory device comprising:

a conductive bottom electrode;

a multi-resistive state element arranged on top of and in contact with the bottom electrode such that a bottom interface Is created, the multi-resistive state element having at least one layer that is fabricated to be substantially crystalline and have a programmable resistance; and

a conductive top electrode arranged on top of and in contact with the multi-resistive state element such that a top interface is created;

wherein the resistance of the resistive memory device may be programmed by applying a first voltage having a first polarity across the conductive electrodes and reversibly programmed by applying a second voltage having a second polarity across the conductive electrodes; and

wherein at least the top interface or the bottom interface is subjected to a treatment **primarily** directed towards changing properties of the at least one interface.

29. **(Currently Amended)** The resistive memory device of claim ~~27~~ **29** , wherein:

the at least one layer that is fabricated to be substantially crystalline is fabricated to be polycrystalline.

30. **(Currently Amended)** The resistive memory device of claim ~~27~~ **29**, wherein:

the at least one layer that is fabricated to be substantially crystalline is fabricated to be a perovskite.

31. **(Currently Amended)** The resistive memory device of claim ~~29~~ **30**, wherein:

the interface that is subjected to a treatment is directed towards changing the properties of the perovskite.